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042/63/25
eSRAM team / Crolles1

1.Goal of the meeting

The main topics for the meeting are:

- Status on current tasks:
  - T2.4: Abstractor prototype (LIP6)
  - T3.2: Model-checking with optimized timed automaton (LSV)
  - T3.3: Verification prototype (LSV)
- Status on deliverables T0+18:
  - T3.2: Model-checking with optimized timed automaton (LSV)
- Document to provide to the ANR T0+18:
  - Each partner: Provide summary document and the cost of the project for this period
- Prepare meeting with the ANR planned for the 12th September: each partner have to provide 10 slides with his collaboration to the project for the 18 first months of the project

2.Attendees

Patricia Renault	LIP6
Emmanuelle Encrenaz	LIP6
Pirouz Bazargan-Sabet	LIP6
Dominique Ledu	LIP6
Laurent Fribourg	LSV
Etienne André	LSV
Remy Chevallier	ST

3.Summary of the meeting

3.1.Communication with the ANR: status on 'accord de consortium'

No progress. Need a feedback from the lawyer department in ST and CEA

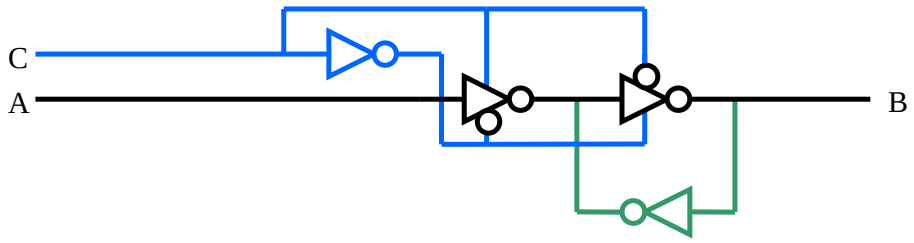
3.2.Status on Deliverables

3.2.1.T2.4: Abstractor prototype (LIP6)

- Pattern matching algorithm has been studied by 2 trainees. Signature and branch algorithms are developed. However, a case is not supported, thus the algorithm must be improved.
- Color algorithm implemented in the abstractor prototype: Abstraction performed in SPSMALL in few seconds (between 6s and 40s depending on net list parsing strategy)
- Next: Try to solve loop conflicts automatically (mainly eSRAM memory points) by a dedicated algorithm

3.2.2.T3.2: Temporal automaton model checking adapted to memory D3.2 (LIP6)

- Spice simulation runs on each gate is included in the abstractor prototype
- However in dedicated cases, few elementary bricks must be plugged together in order to run the timing simulation and provide a consistent model



The transistor abstraction prototype generates the 3 elementary bricks in blue, black and green. The timing analysis of each brick independently does not make sense. The analysis of the complete structure is mandatory.

- Next: build automatically the complex bricks and run the transistor based simulation on them.

3.2.3.T3.3: Verification prototype (LSV)

- The verification prototype generates automatically the timed automaton for VHDL instantiations. The VDHL process is not supported today.
- With this prototype, the 'trial before study1' and a part of the study1 have been verified as following:
  - According to the specification behavioral constraints (ie what is a write/read cycle) and timing constraints (cycle time…) are modeled.
  - The verification tool Hytech, generates the next step from a working one, and lists the behaviors which do not follow the behavioral and/or the timing constraints.
  - The behaviors, which are not allowed, induce additional constraints on parameters (setup, hold, cycle time, access time).
  - The additional constraints must be compared to the timings in the specification in order to know if the design performances are improved or not.
- Next: use the prototype on a complete SPSMALL of one word of one bit.

3.3.Prepare review with ANR planned the 11th September in Paris

- First draft for the slides has been presented by LIP6 and ST. A global presentation of 40 minutes is planned for the review

4.Actions

- Administrative
  - Follow-up the 'Accord de consortium' story (All) [asap]

  - Provide the summary document (All) [end June]
  - Provide the cost document (All) [end June]
- Prototypes development
  - Loop analysis (LIP6) [September 2008]
  - Delay computation (LIP6) [September 2008]
  - Run verification prototype on full SPSMALL with one word of one bit (LSV) [September 2008]
  - Provide deliverable D3.2 (LSV) [September 2008]
  - Support generated process statement in VHDL (LSV) [September 2008]
- Prepare ANR meeting in September
  - Provide summary of the work performed (All) [week 27]
- Prepare paper for DATE. First planned provided by email (LSV) [week 24]

5.Next meeting

The next meeting is planned at ST office in Crolles during week 35.

6.Deliverable overview

No.	Title	Deliv.	Resp.	Target	status
D1.1	State of Art in eSRAM conception	R	ST	0→6	done
D1.2	Build web site for the project	R	LIP6	0→6	done
D1.3	Description of the conception flow applied on a study	R	ST	6→12	Study 1 done Study 2 done Study 3 not started Run time of conception flow done
D2.1	State of art in memory verification methodologies	R	LIP6	0→6	done
D2.2	Definition of a new functional and timed model	R	LIP6	0→6	done
D2.3	Mixing of abstraction methods and temporal characterization	R	LIP6	6→12	done
D2.4	Abstraction tool prototype	P	LIP6	12→24	ongoing
D3.1	Temporal automaton modeling adapted to memory	R	LSV	6→12	done
D3.2	Temporal automaton model checking adapted to memory	R	LSV	12→18	ongoing
D3.3	verification tool prototype	P	LSV	12→24	ongoing
~~D4.1~~	~~Description of the conception flow applied on other studies~~	~~R~~	~~ST~~	~~12→18~~	~~Not started~~
D4.2	Experimentation of prototypes on real study	R & D	ST	18→36	Not stated
D4.3	Comparison of results from current verification methods and new methods	R	ST	30→36	Not started

The targets are described in months.
Delivery naming: (R: report / P: prototype / D: demonstrator)
wk: week number
Q: quarter