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1.Goal of the meeting

The aims of the meeting are to:

- Status of deliverables
- Define technical interface between partners
- Status of the modeling of the SPSMALL by LIP6

The meeting has been done at ST office in Crolles the 4th July 2007.

2.Attendees

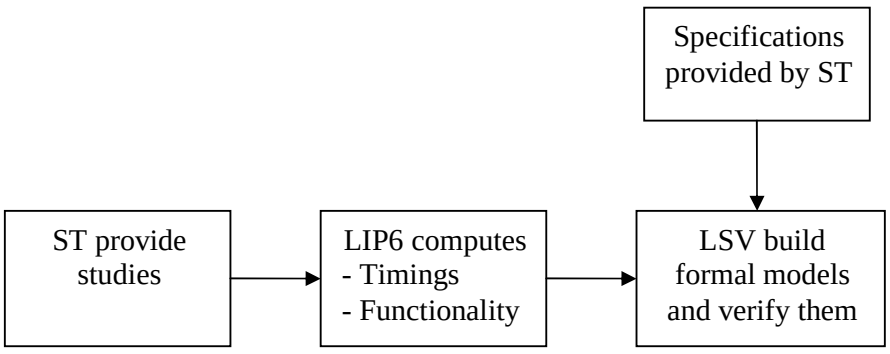
Emmanuelle Encrenaz	LSV/LIP6
Pirouz Bazargan-Sabet	LIP6
Laurent Fribourg	LSV
Remy Chevallier	ST

3.Summary of the meeting

3.1.Status of deliverables

- D1.1 delivery 'State of Art in eSRAM conception' is updated and finished by ST
- The SPSMALL study provided by ST has been read by the LIP6 all the needed data has been provided
- Verification part of D2.1 delivery 'State of art in memory verification' has been updated and finished by LSV
- First release of abstraction part for D2.1 delivery 'State of art in memory verification' has been provided by LIP6
- A common first page for each delivery will be written before providing them through the web-site of the project

3.2.Define technical interface between partners



Targeted data flow between partners when the automation step will be done

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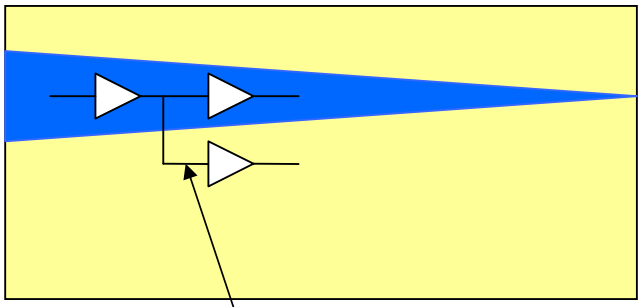
3.2.1.ST / LIP6

For the Study1, ST provides schematics by print-screen mechanism. For the Study2, this way cannot be used because the complexity of the SPREG does not allow it. However, LIP6 has Cadence licenses. In this case, ST will provide the schematics through Opus database.

3.2.2.LIP6 / LSV

The communication flow between LIP6 and LSV is under-definition.
In a first step, timings and abstraction will be provided manually, and the LSV will use it by hand in order to define definitive file formats.
However, we have decided that the abstracted model must be simplified in order to allow the formal engine to verify it as quick as possible. The simplification will be done after the abstraction because the delays induced by all the loads must be taken into account. This step will be performed according to the properties.



The logic gate has to be removed for the property checking step but the loads induced by this gate have to be kept

Complete design

Part of the design which rely on the properties to check

In the abstraction part of the D2.1 document provided by LIP6, 3 timing models have been defined:

1. Max delays for each transition (output go from 0 to 1 and from 1 to 0)
2. Max delays for the transistor of a given input (worst case for the other inputs)
3. All the transitions are described including multi-toggling of inputs

We decided that, in a first step, a model between (2) and (3) will be used. This model will describe all the cases except the multi-toggling cases. Indeed, we model timings, thus this case cannot occurs.
This choice will be described and discussed in delivery D2.2 by LIP6.

4.Actions

- Provide a common first page for all the deliverable (Emmanuelle) [week41]
- Provide a draft of D2.2 deliverable (Pirouz, Emmanuelle, Laurent) [week41]

- Evaluate manually the new timed model on the SPSMALL (Emmanuelle, Laurent) [week41]
- Continue the abstraction of the first study (Pirouz) [week41]
- Provide a first release for the study2 (Remy) [week41]
- Provide intermediate report to Laurent Fribourg (Pirouz, Remy) [week28]
- Communication task: **a public web-site will be developed** and managed by the LSV and the D1.1 and D2.1 will be put in it.

5.Next meeting

The next meeting is planned in Paris at the LIP6 office the 12th October 2007.

6.Deliverable overview

No.	Title	Deliv.	Resp.	Target	status
D1.1	State of Art in eSRAM conception	R	ST	0→6	done
D1.2	Studies definitions	R	ST	0→6	Study 1 done Study 2 ongoing (wk41)
D1.3	Description of the conception flow applied on a study	R	ST	6→12	Not started
D2.1	State of art in memory verification methodologies	R	LIP6	0→6	done
D2.2	Definition of a new functional and timed model	R	LIP6	0→6	Draft version planned (wk41)
D2.3	Mixing of abstraction methods and temporal characterization	R	LIP6	6→12	Not started
D2.4	Abstraction tool prototype	P	LIP6	12→24	Not started
D3.1	Temporal automaton modeling adapted to memory	R	LSV	6→12	Not started
D3.2	Temporal automaton model checking adapted to memory	R	LSV	12→18	Not started
D3.3	verification tool prototype	P	LSV	12→24	Not started
D4.1	Description of the conception flow applied on other studies	R	ST	12→18	Not started
D4.2	Experimentation of prototypes on real study	R & D	ST	18→36	Not stated
D4.3	Comparison of results from current verification methods and new methods	R	ST	30→36	Not started

The targets are described in months.
Delivery naming: (R: report / P: prototype / D: demonstrator)
wk: week number
Q: quarter