# Functional and Timing Abstraction

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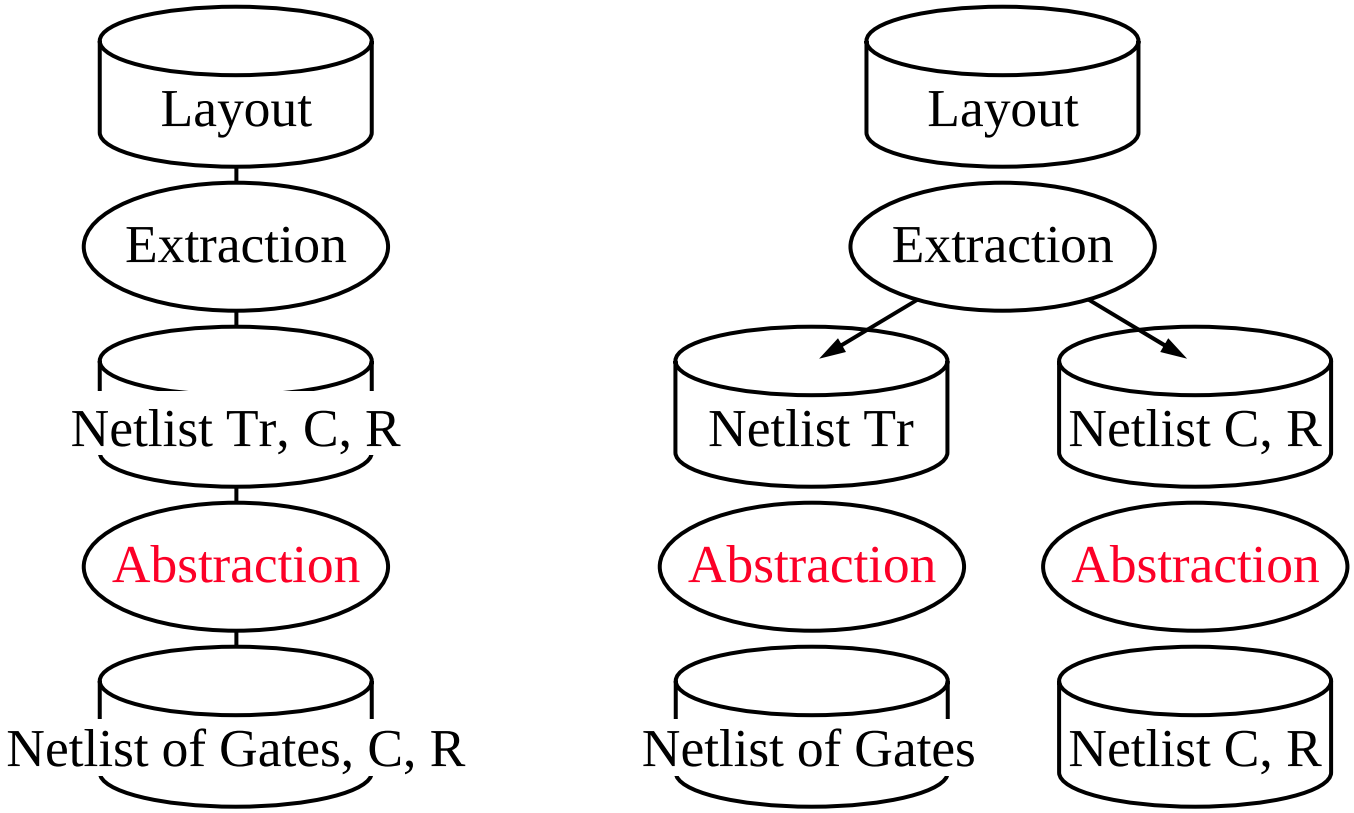
# Outline

- Functional Abstraction
- Timing Model
- Delay Evaluation

# Introduction



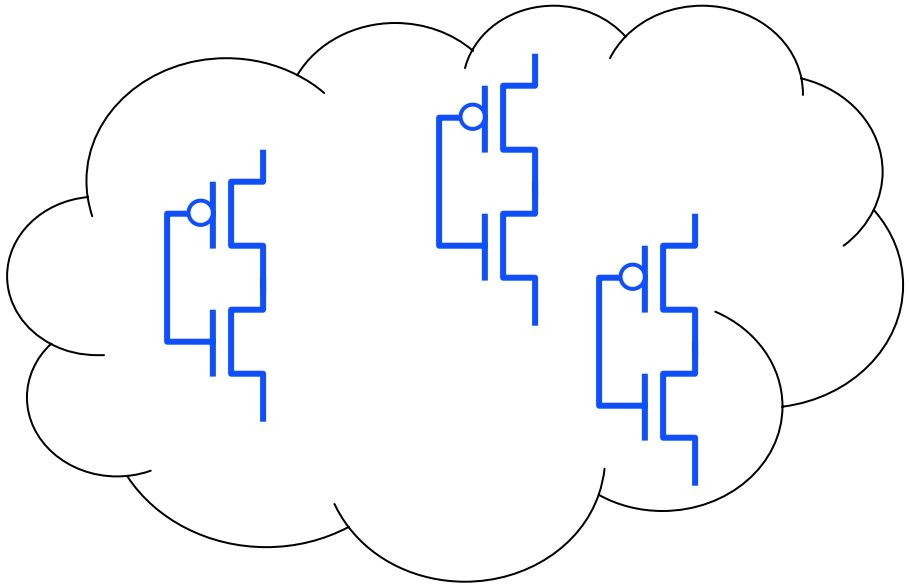
# Functional Abstraction

Aim :

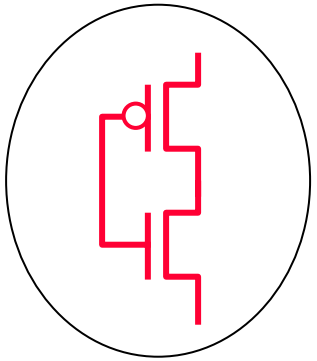
Recongnize gates from transistors network

# Functional Abstraction

Classic Method : Pattern Matching



circuit



pattern

# Functional Abstraction

Classic Method : Pattern Matching

⊕ Classic algorithm

Speed up using signature comparison

⊖ Require to know the circuit

Not adapted to custom designs

Does not respect the electrical point of view

# Functional Abstraction

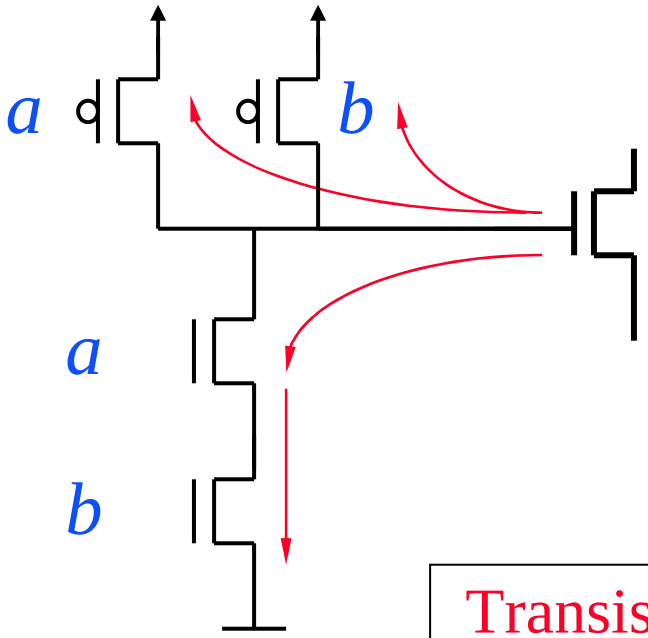
Formal Method

Recognize the *function* of a transistor structure

Electrical point of view - Current trace

# Functional Abstraction

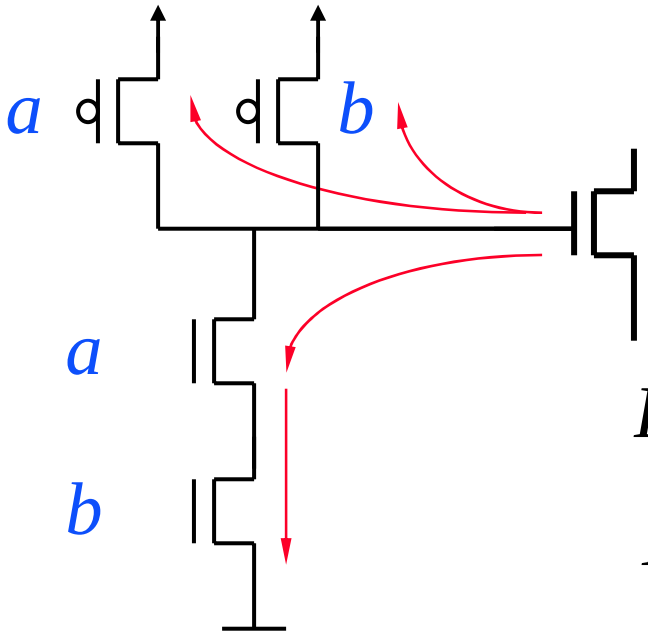
follow the current paths




Transistor structure is not enough

Functional analysis is required

# Functional Abstraction

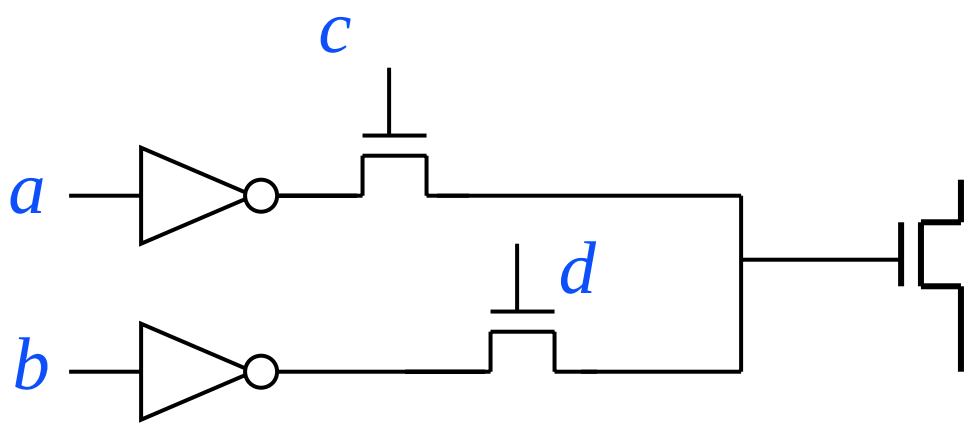



$$F_{up} = \bar{b} + \bar{a}$$

$$F_{down} = a \cdot b$$

$$F_{up} = \overline{F_{down}}$$

# Functional Abstraction




$$F_{up} = \overline{a}.c + \overline{b}.d$$

$$F_{down} = a.c + b.d$$

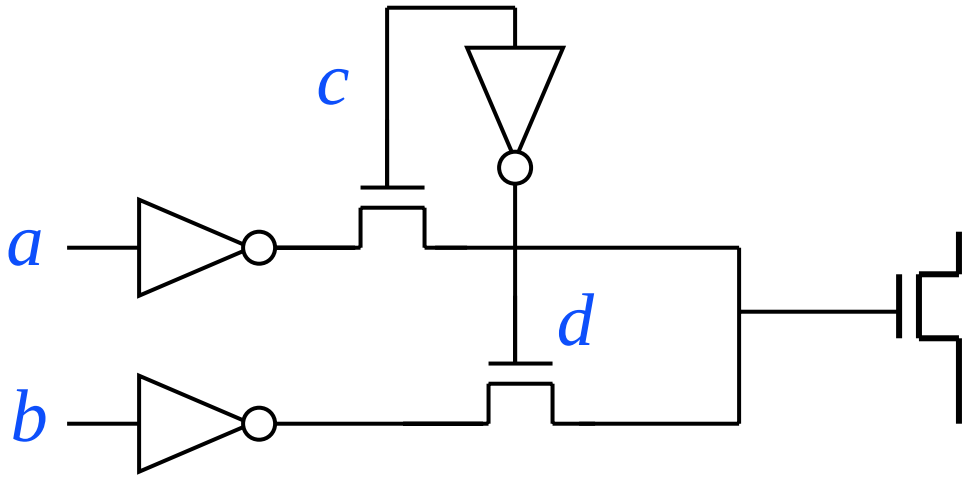
$$F_{up} \,.\, F_{down} = c.d.(a \oplus b)$$

conflict

$$\overline{F_{up} + F_{down}} = \overline{c}.\overline{d}$$

tri-state

# Functional Abstraction




$c = \overline{d}$

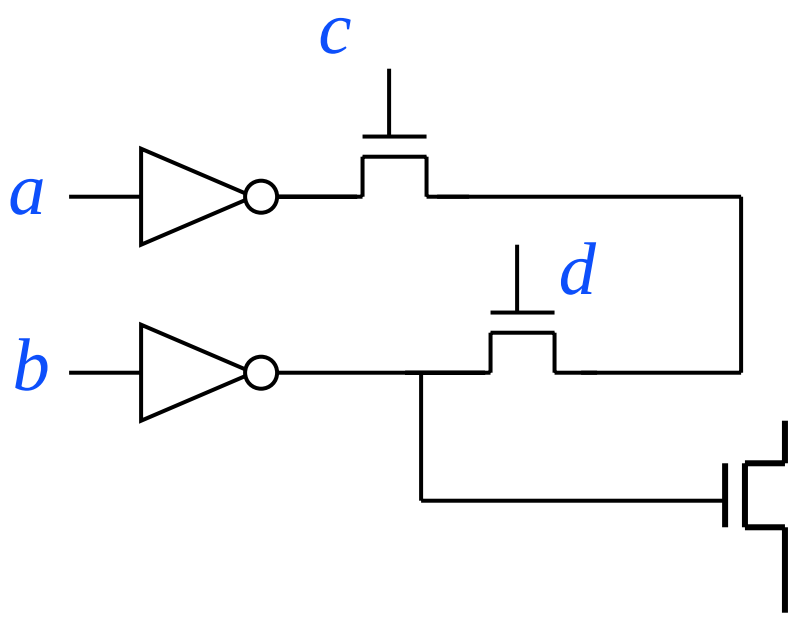
$$F_{up} \cdot F_{down} = c.d.(a \oplus b)$$

$$\overline{F_{up} + F_{down}} = \overline{c}.\overline{d}$$

conflict

tri-state

# Functional Abstraction



# Functional Abstraction

Formal Method : problems

How far I have to explore ?

Apparition of loops

# Functional Abstraction

Formal Method : Loops

A loop is the signature of a memory point

Break point in the backward exploration

# Functional Abstraction

Formal Method : Identifying a memory point

$$x_i = f(x_1, \ldots, x_i, \ldots, x_n) = x_i \cdot \overline{f_{i1}} + x_i \cdot f_{i0}$$

$$\frac{\partial f}{\partial x_i} = f_{i0} \; xor \; f_{i1} = \overline{f_{i1}} \cdot f_{i0} + f_{i1} \cdot \overline{f_{i0}}$$

$\overline{f_{i1}} \cdot f_{i0}$ and $f_{i1} \cdot \overline{f_{i0}}$ cannot be **1** for a given input configuration

# Functional Abstraction

Formal Method : Identifying a memory point

$$f = x_i \cdot f_{i1} + \overline{x_i} \cdot f_{i0}$$

if $f_{i1} \cdot \overline{f_{i0}}\,(v) = 1$, $f$ varies in direct way with $x_i$

$f$ is a positive function of $x_i$

if $\overline{f_{i1}} \cdot f_{i0}\,(v) = 1$, $f$ varies in opposite way with $x_i$

$f$ is a negative function of $x_i$

$$\frac{\partial f^{+}}{\partial x_i} = f_{i1} \cdot \overline{f_{i0}}$$

$$\frac{\partial f^{-}}{\partial x_i} = \overline{f_{i1}} \cdot f_{i0}$$

# Functional Abstraction

Formal Method : Identifying a memory point

$$f = x_i \cdot f_{i1} + \overline{x_i} \cdot f_{i0}$$

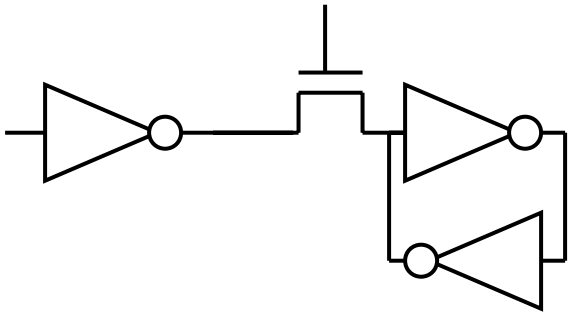
for a memory point

$$\frac{\partial f^{+}}{\partial x_i} = f_{i1} \cdot \overline{f_{i0}} \neq 0 \qquad \frac{\partial f^{-}}{\partial x_i} = \overline{f_{i1}} \cdot f_{i0} \equiv 0$$

# Functional Abstraction

## Formal Method : Identifying a memory point

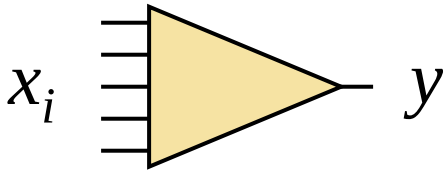
Formal analysis cannot identify memory points
usig electrical conflicts



# Outline

- Functional Abstraction
- Timing Model
- Delay Evaluation

# Timing Model



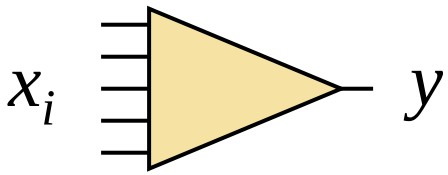

How to abstract each gate from the timing point of view

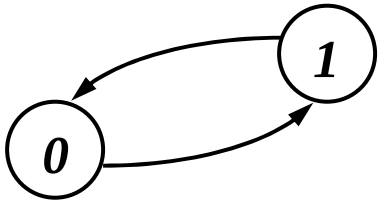
STG (State Transition Graph)

# Timing Model

Unique delay model

consider the transitions of $y$



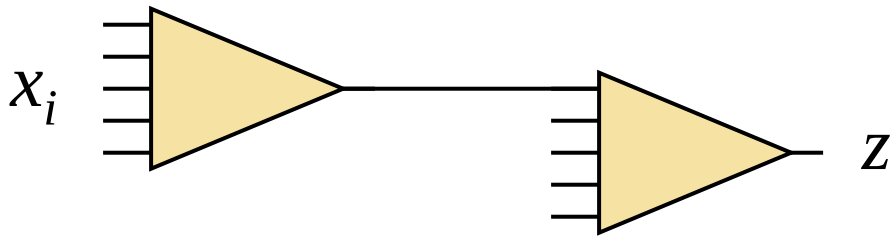




the worst case delay is attributed to each transition

# Timing Model

Unique delay model

worst case delays cannot be summed



# Timing Model

Input-output delay model

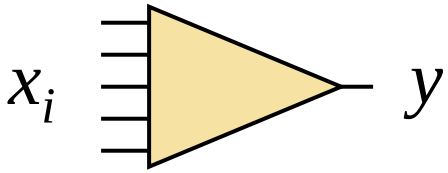
consider the transitions of *y with respect to xi*

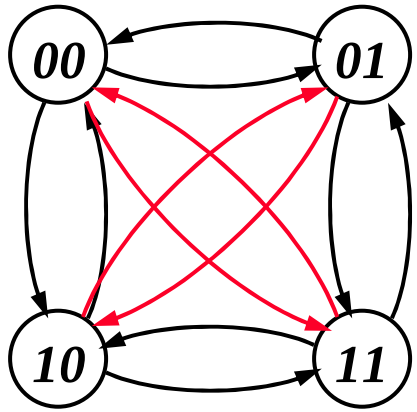
N 4-state graphs for an N-input gate

# Timing Model

Input-output delay model

consider the transitions of *y with respect to xi*



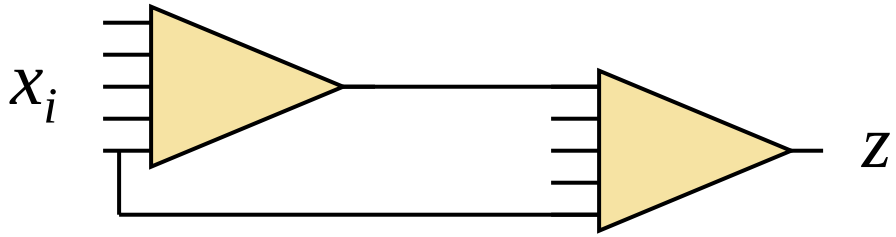




the worst case delay is attributed to each transition

# Timing Model

Input-output delay model

worst case delays cannot be summed in case of correlations



# Timing Model

Complete STG delay model

consider the transitions of *y with respect to the transition of the configuration xi*

1 $2^N$-state graph for an N-input gate

# Outline

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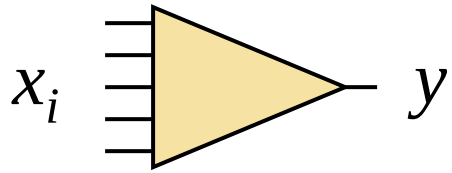
# Delay Evaluation

How to characterize the delay of a transition

# Delay Evaluation

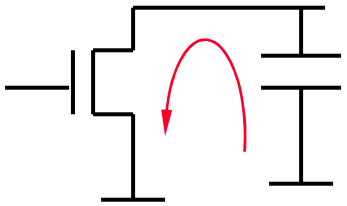
Accurate delay using electrical simulation




Electrical simulation (Spice) of each configuration

# Delay Evaluation

Analytic delay using a transistor model



$$i_{ds} = -C\frac{dv}{dt}$$

choose a transistor model ($i_{ds}$) and resolve the differential equation